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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W., Suite 600
Washington, DC 20036-5339

EXAMINER	
YIGDALL, MICHAEL J	

ART UNIT	PAPER NUMBER
2122	2

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 09/964,369	Applicant(s) IGA, KIICHIRO	
	Examiner Michael J. Yigdall	Art Unit 2122	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondenc address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 are pending and have been examined. The priority date considered for the application is 11 May 2001.

Drawings

2. The drawings are objected to because of the following informalities: Figure 3 contains typographical errors such as "Newest *Branthing* Destination Address" and "*8st* Branching Address 0" (emphasis added). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract of the disclosure is objected to because the abstract must not exceed 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4, 7-9 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,633,973 to Kanzaki.

With respect to claim 1, Kanzaki discloses a method for generating trace information of an information processing device (see the title and abstract), wherein the information processing device includes a processing unit and an interface device (see column 7, lines 1-9, which shows a CPU and an interface device for output), wherein the processing unit generates operational information when branching occurs during processing (see column 7, lines 19-26, which shows the CPU generating a control signal when branching occurs), and wherein the interface device has a buffer circuit for receiving the operational information of the branching from the processing unit (see column 7, lines 1-9, which shows a trace memory or buffer for storing event information), the method comprising the steps of:

(a) generating an absolute branching destination address each time a branching occurs when the processing unit performs processing (see column 7, lines 27-30, which shows generating a branching destination address when branching occurs, and column 8, lines 38-46, which further shows generating an absolute branching destination address);

(b) storing the absolute branching destination address in the buffer circuit (see column 7, line 63 to column 8, line 6, which shows storing the branching destination address in the trace memory or buffer);

(c) generating a flag based on the absolute branching destination address (see column 7, lines 19-26, which shows generating a status flag based on a branching event); and

(d) storing the flag in the buffer circuit in association with the absolute branching destination address (see column 7, line 63 to column 8, line 6, which shows storing the status flag in the trace memory or buffer in association with the branching destination address).

Kanzaki discloses generating an absolute branching destination address based on a relative address (see column 8, lines 38-46), but does not expressly disclose the step of:

(e) generating a relative branching destination address based on the stored absolute branching destination address.

However, the correlation between an absolute address and a relative address is known in the art, and it is known that one such address can be determined based on the other (for example, see Kanzaki, column 8, lines 38-46). Kanzaki also shows that a fewer number of bits are needed to represent a relative address than for an absolute address (see column 8, lines 14-21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Kanzaki to generate a relative branching destination address based on an absolute address, as is known in the art, in order to represent the address using a fewer number of bits.

Kanzaki further discloses the step of:

(f) outputting, based on the flag, either one of the absolute branching destination address and the relative branching destination address (see column 8, lines 14-21, which shows outputting the status flag and the branching destination address).

With respect to claim 4, Kanzaki discloses an information processing device (see the title and abstract) comprising:

(a) a processing unit for generating a branching occurrence signal and an absolute branching destination address each time a branching occurs during processing (see CPU 2 in FIG. 7 and column 7, lines 19-30, which shows the CPU generating a control signal and a

branching destination address when branching occurs, and column 8, lines 38-46, which further shows generating an absolute branching destination address);

(b) a determination circuit connected to the processing unit for comparing a formerly generated absolute branching destination address and a subsequently generated absolute branching destination address and generating a flag in accordance with comparison result (see circuit 31 in FIG. 1 and column 7, lines 27-30, which shows determining the generated address, and column 7, lines 19-26, which shows generating an associated status flag);

(c) a buffer circuit connected to the processing unit and the determination circuit for sequentially associating the absolute branching destination address with the flag, sequentially storing the associated absolute branching destination address and the flag, and outputting the absolute branching destination address and the flag in order stored (see trace memory 43 in FIG. 1 and column 7, lines 1-9, which shows a buffer for storing event information; see also column 7, line 63 to column 8, line 6, which shows storing the branching destination address and the status flag in the buffer, and column 8, lines 14-21, which shows outputting the status flag and the branching destination address, in order); and

(d) an output circuit connected to the buffer circuit, wherein the output circuit outputs, based on the flag, either one of the absolute branching destination address and the relative branching destination address (see trace circuit 44 in FIG. 1 and column 8, lines 14-21, which shows outputting the status flag and the branching destination address).

Kanzaki discloses generating an absolute branching destination address based on a relative address (see column 8, lines 38-46), but does not expressly disclose the limitation of part

(d) above wherein the output circuit is for generating a relative branching destination address based on the stored absolute branching destination address.

However, the correlation between an absolute address and a relative address is known in the art, and it is known that one such address can be determined based on the other (for example, see Kanzaki, column 8, lines 38-46). Kanzaki also shows that a fewer number of bits are needed to represent a relative address than for an absolute address (see column 8, lines 14-21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Kanzaki to generate a relative branching destination address based on an absolute address, as is known in the art, in order to represent the address using a fewer number of bits.

With respect to claim 7, Kanzaki discloses computing an absolute value based on a formerly generated absolute address and a subsequently generated relative address received from the processing unit (see column 8, lines 38-46), but does not expressly disclose the limitation wherein the determination circuit computes a relative value between the formerly generated absolute branching destination address which is most recently stored in the buffer circuit and the subsequently generated absolute branching destination address received from the processing unit.

However, the correlation between an absolute address and a relative address is known in the art, and it is known that one such address can be determined based on the other (for example, see Kanzaki, column 8, lines 38-46). Kanzaki also shows that a fewer number of bits are needed to represent a relative address than for an absolute address (see column 8, lines 14-21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Kanzaki to compute a relative branching destination

address based on absolute addresses, as is known in the art, in order to represent the address using a fewer number of bits.

Although Kanzaki further discloses outputting the status flag and the branching destination address (see column 8, lines 14-21), Kanzaki does not expressly disclose the limitation wherein the determination circuit generates a first flag to output the absolute branching destination address from the output circuit when the relative value is included in a predetermined range, and generates a second flag to output the relative branching destination address from the output circuit when the relative value is not included in the predetermined range.

However, flags generated as a result of a computation are well known in the art. For example, it is known that an overflow bit or flag may be set when a computed value is outside of a predetermined range. When the computed value is within the predetermined range, the overflow flag would be cleared, or an alternative flag may be set. An example of such a predetermined range known in the art is the range of values that may be represented using a given number of bits.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to generate flags in the Kanzaki system, in order to indicate, for example, whether the address computation (see column 8, lines 38-46) resulted in an overflow condition.

With respect to claim 8, Kanzaki further discloses the limitation wherein the output circuit includes:

(a) an absolute address buffer connected to the buffer circuit for storing a first absolute branching destination address received from the buffer circuit (see column 7, line 63 to column

8, line 6, which shows storing the branching destination address in the trace memory or buffer; see also column 8, lines 23-25, which shows storing absolute addresses).

Kanzaki discloses computing an absolute branching destination address by subtracting a second relative address from a first absolute address (see column 8, lines 38-46), but does not expressly disclose:

(b) a subtraction circuit connected to the absolute address buffer and the buffer circuit for computing an relative branching destination address using the first absolute branching destination address and a second absolute branching destination address, which is next output from the buffer circuit after the first absolute branching destination address.

However, the correlation between an absolute address and a relative address is known in the art, and it is known that one such address can be determined based on the other (for example, see Kanzaki, column 8, lines 38-46). Kanzaki also shows that a fewer number of bits are needed to represent a relative address than for an absolute address (see column 8, lines 14-21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Kanzaki to compute a relative branching destination address based on absolute addresses, as is known in the art, in order to represent the address using a fewer number of bits.

Kanzaki further discloses:

(c) a relative address buffer connected to the subtraction circuit for storing the relative branching destination address (see column 7, line 63 to column 8, line 6, which shows storing the branching destination address in the trace memory or buffer; see also column 8, lines 23-25, which shows storing relative addresses); and

(d) a serial-conversion circuit connected to the absolute address buffer and the relative address buffer for serial-converting either one of the first absolute branching destination address and the relative branching destination address and for thereafter outputting the serial-converted branching destination address (see column 8, lines 7-21, which shows outputting the branching destination address sequentially on a 4-bit terminal in tune with clock and synchronization signals, which constitutes serial conversion).

With respect to claim 9, Kanzaki discloses an information processing device (see the title and abstract) comprising:

(a) a processing unit for generating a branching occurrence signal, an absolute branching destination address, and a command fetch number each time a branching occurs during processing (see CPU 2 in FIG. 7 and column 7, lines 19-30, which shows the CPU generating a control signal and a branching destination address when branching occurs, and column 8, lines 38-46, which further shows generating an absolute branching destination address; see also column 8, lines 33-37, which shows generating an opcode or command fetch number);

(b) a determination circuit connected to the processing unit for comparing a formerly generated absolute branching destination address and a subsequently generated absolute branching destination address and generating a flag in accordance with comparison result (see circuit 31 in FIG. 1 and column 7, lines 27-30, which shows determining the generated address, and column 7, lines 19-26, which shows generating an associated status flag); and

(c) a buffer circuit connected to the processing unit and the determination circuit for associating the absolute branching destination address with the flag, sequentially storing the associated absolute branching destination address and the flag, and outputting the absolute

branching destination address and the flag in order stored (see trace memory 43 in FIG. 1 and column 7, lines 1-9, which shows a buffer for storing event information; see also column 7, line 63 to column 8, line 6, which shows storing the branching destination address and the status flag in the buffer, and column 8, lines 14-21, which shows outputting the status flag and the branching destination address, in order).

Although Kanzaki discloses a command fetch number (see column 8, lines 33-37), Kanzaki does not expressly disclose the limitation of part (c) above wherein the command fetch number is associated with the absolute branching destination address, sequentially stored, and output in the order stored.

However, Kanzaki does disclose storing an associated status flag with the branching destination address (see column 7, line 63 to column 8, line 6) and outputting the address and flag in sequential order (column 8, lines 14-21), for the purpose of informing an external debugger of a branch trace event (see column 7, lines 19-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store and output the command fetch number along with the status flag, in the Kanzaki system, for the purpose of providing the additional trace event information to an external debugger.

Kanzaki further discloses:

(d) an output circuit connected to the buffer circuit, wherein the output circuit outputs, based on the flag, either one of the absolute branching destination address and the relative branching destination address (see trace circuit 44 in FIG. 1 and column 8, lines 14-21, which shows outputting the status flag and the branching destination address).

Kanzaki discloses generating an absolute branching destination address based on a relative address (see column 8, lines 38-46), but does not expressly disclose the limitation of part (d) above wherein the output circuit is for generating a relative branching destination address based on the stored absolute branching destination address.

However, the correlation between an absolute address and a relative address is known in the art, and it is known that one such address can be determined based on the other (for example, see Kanzaki, column 8, lines 38-46). Kanzaki also shows that a fewer number of bits are needed to represent a relative address than for an absolute address (see column 8, lines 14-21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Kanzaki to generate a relative branching destination address based on an absolute address, as is known in the art, in order to represent the address using a fewer number of bits.

Although Kanzaki further discloses a command fetch number (see column 8, lines 33-37), Kanzaki does not expressly disclose the limitation of part (d) above wherein the output circuit outputs the command fetch number.

However, Kanzaki does disclose outputting the branching destination address and a status flag (see column 8, lines 14-21), for the purpose of informing an external debugger of a branch trace event (see column 7, lines 19-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to output the command fetch number along with the status flag, in the Kanzaki system, for the purpose of providing the additional trace event information to an external debugger.

With respect to claim 12, Kanzaki discloses computing an absolute value based on a formerly generated absolute address and a subsequently generated relative address received from the processing unit (see column 8, lines 38-46), but does not expressly disclose the limitation wherein the determination circuit computes a relative value between the formerly generated absolute branching destination address which is most recently stored in the buffer circuit and the subsequently generated absolute branching destination address received from the processing unit.

However, the correlation between an absolute address and a relative address is known in the art, and it is known that one such address can be determined based on the other (for example, see Kanzaki, column 8, lines 38-46). Kanzaki also shows that a fewer number of bits are needed to represent a relative address than for an absolute address (see column 8, lines 14-21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Kanzaki to compute a relative branching destination address based on absolute addresses, as is known in the art, in order to represent the address using a fewer number of bits.

Although Kanzaki further discloses outputting the status flag and the branching destination address (see column 8, lines 14-21), Kanzaki does not expressly disclose the limitation wherein the determination circuit generates a first flag to output the absolute branching destination address from the output circuit when the relative value is included in a predetermined range, and generates a second flag to output the relative branching destination address from the output circuit when the relative value is not included in the predetermined range.

However, flags generated as a result of a computation are well known in the art. For example, it is known that an overflow bit or flag may be set when a computed value is outside of

a predetermined range. When the computed value is within the predetermined range, the overflow flag would be cleared, or an alternative flag may be set. An example of such a predetermined range known in the art is the range of values that may be represented using a given number of bits.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to generate flags in the Kanzaki system, in order to indicate, for example, whether the address computation (see column 8, lines 38-46) resulted in an overflow condition.

With respect to claim 13, Kanzaki further discloses the limitation wherein the output circuit includes:

(a) an absolute address buffer connected to the buffer circuit for storing a first absolute branching destination address received from the buffer circuit (see column 7, line 63 to column 8, line 6, which shows storing the branching destination address in the trace memory or buffer; see also column 8, lines 23-25, which shows storing absolute addresses).

Kanzaki discloses computing an absolute branching destination address by subtracting a second relative address from a first absolute address (see column 8, lines 38-46), but does not expressly disclose:

(b) a subtraction circuit connected to the absolute address buffer and the buffer circuit for computing a relative branching destination address using the first absolute branching destination address and a second absolute branching destination address, which is next output from the buffer circuit after the first absolute branching destination address.

However, the correlation between an absolute address and a relative address is known in the art, and it is known that one such address can be determined based on the other (for example,

see Kanzaki, column 8, lines 38-46). Kanzaki also shows that a fewer number of bits are needed to represent a relative address than for an absolute address (see column 8, lines 14-21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Kanzaki to compute a relative branching destination address based on absolute addresses, as is known in the art, in order to represent the address using a fewer number of bits.

Kanzaki further discloses:

(c) a relative address buffer connected to the subtraction circuit for storing the relative branching destination address (see column 7, line 63 to column 8, line 6, which shows storing the branching destination address in the trace memory or buffer; see also column 8, lines 23-25, which shows storing relative addresses); and

(d) a serial-conversion circuit connected to the absolute address buffer and the relative address buffer for serial-converting the command fetch number, outputting the serial-converted command fetch number, serial-converting either one of the first absolute branching destination address and the relative branching destination address, and outputting the serial-converted branching destination address (see column 8, lines 7-21, which shows outputting the branching destination address sequentially on a 4-bit terminal in tune with clock and synchronization signals, which constitutes serial conversion).

With respect to claim 14, see the explanation for claim 4 set forth above. Claim 14 is recited as an information processing system that is substantially equivalent to the information processing device recited in claim 4.

6. Claims 2, 3, 5, 6, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanzaki, as applied to claims 1, 4 and 9 above, respectively, in view of U.S. Pat. No. 5,809,293 to Bridges et al. (hereinafter Bridges).

With respect to claim 2, Kanzaki does not expressly disclose the steps of:

(a) deleting a predetermined absolute branching destination address stored in the buffer circuit when the absolute branching destination addresses fully occupy the buffer circuit; and

(b) shifting the flag associated with the deleted predetermined absolute branching destination address to output the absolute branching destination address.

However, Bridges discloses steps (a) and (b) above in terms of a first in, first out queue (see column 2, lines 29-40) for storing trace address information (see column 4, lines 61-64). The addresses stored in the FIFO buffer are output to a serialization circuit (see column 7, line 59 to column 8, line 5); when the FIFO buffer is full, addresses are shifted and deleted from the queue one at a time to output the data (see column 7, lines 18-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to delete an address from the Kanzaki buffer and shift the contents of the buffer when it is full to output that address, as taught by Bridges, in order to effectively prevent any stalling of the processor (see Bridges, column 8, lines 3-5).

With respect to claim 3, Kanzaki further discloses the steps of:

(a) based on the flag, serial-converting either one of the absolute branching destination address and the relative branching destination address (see column 8, lines 7-21, which shows

outputting the branching destination address sequentially on a 4-bit terminal in tune with clock and synchronization signals, which constitutes serial conversion); and

(b) outputting the serial-converted branching destination address (see column 8, lines 7-21, which shows outputting the branching destination address sequentially or serially on a 4-bit terminal in tune with clock and synchronization signals).

With respect to claim 5, Kanzaki does not expressly disclose a control circuit connected to the processing unit, the determination circuit, and the buffer circuit for deleting a predetermined absolute branching destination address stored in the buffer circuit when the absolute branching destination addresses fully occupy the buffer circuit and for shifting the flag associated with the deleted predetermined absolute branching destination address to output the absolute branching destination address from the output circuit.

However, Bridges discloses the feature above in terms of a first in, first out queue (see column 2, lines 29-40) for storing trace address information (see column 4, lines 61-64). The addresses stored in the FIFO buffer are output to a serialization circuit (see column 7, line 59 to column 8, line 5); when the FIFO buffer is full, addresses are shifted and deleted from the queue one at a time to output the data (see column 7, lines 18-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a control circuit in the system of Kanzaki for deleting an address from the buffer and for shifting the contents of the buffer when it is full to output that address, as taught by Bridges, in order to effectively prevent any stalling of the processor (see Bridges, column 8, lines 3-5).

With respect to claim 6, Kanzaki does not expressly disclose the limitation wherein the control circuit generates relative branching occurrence state information or absolute branching occurrence state information based on the branching occurrence signal and the flag and generates address deletion state information when an address in the buffer circuit is deleted.

However, Bridges discloses the limitations above in terms of generating state information based on a branch occurrence (see column 8, lines 11-26) and generating state information when an address in the FIFO buffer is output, i.e. deleted from the buffer (see column 7, lines 48-56). Such state information enables a user to trace the flow of execution within the processor, including any branches that have occurred (see column 5, lines 41-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate the state information taught by Bridges in the system of Kanzaki, for the purpose of enabling a user to trace the flow of execution within the processor.

With respect to claim 10, Kanzaki does not expressly disclose a control circuit connected to the processing unit, the determination circuit, and the buffer circuit for deleting a predetermined absolute branching destination address stored in the buffer circuit when the absolute branching destination addresses fully occupy the buffer circuit and for shifting the flag associated with the deleted predetermined absolute branching destination address to output the absolute branching destination address from the output circuit.

However, Bridges discloses the feature above in terms of a first in, first out queue (see column 2, lines 29-40) for storing trace address information (see column 4, lines 61-64). The addresses stored in the FIFO buffer are output to a serialization circuit (see column 7, line 59 to

column 8, line 5); when the FIFO buffer is full, addresses are shifted and deleted from the queue one at a time to output the data (see column 7, lines 18-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a control circuit in the system of Kanzaki for deleting an address from the buffer and for shifting the contents of the buffer when it is full to output that address, as taught by Bridges, in order to effectively prevent any stalling of the processor (see Bridges, column 8, lines 3-5).

With respect to claim 11, Kanzaki does not expressly disclose the limitation wherein the control circuit generates relative branching occurrence state information or absolute branching occurrence state information based on the branching occurrence signal and the flag and generates address deletion state information when an address in the buffer circuit is deleted.

However, Bridges discloses the limitations above in terms of generating state information based on a branch occurrence (see column 8, lines 11-26) and generating state information when an address in the FIFO buffer is output, i.e. deleted from the buffer (see column 7, lines 48-56). Such state information enables a user to trace the flow of execution within the processor, including any branches that have occurred (see column 5, lines 41-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate the state information taught by Bridges in the system of Kanzaki, for the purpose of enabling a user to trace the flow of execution within the processor.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Pat. No. 6,513,134 to Augsburg et al. discloses a system for tracing program execution. U.S. Pat. No. 6,233,678 to Bala discloses a system for profiling programs by collecting a branch history. U.S. Pat. No. 6,009,270 to Mann discloses a system for synchronizing trace records.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (703) 305-0352. The examiner can normally be reached on Monday through Friday from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

Michael J. Yigdall
Examiner
Art Unit 2122

mjy
March 26, 2004

Antony Nguyen-Ba

ANTONY NGUYEN-BA
PRIMARY EXAMINER